DOCKET NO: 204155US2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
KESATOSHI TAKEUCHI, ET AL.	: EXAMINER: WANG, JIN CHENG
SERIAL NO: 09/801,913	:
RCE FILED: NOVEMBER 15, 2004	: GROUP ART UNIT: 2672
FOR: OVERLAY OF PLURAL IMAGES	:

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

The present Appeal Brief is submitted in response to the Final Rejection of September 20, 2005. A Notice of Appeal was timely filed on December 20, 2005.

(i) REAL PARTY IN INTEREST

The real party in interest in the present appeal is Seiko Epson Corporation having a place of business at 4-1, Nishi-shinjuki 2-chome, Shinjuku-ku, Tokyo, Japan.

(ii) RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representatives, and assignee are not aware of any other appeals, interferences, or judicial proceedings that will directly effect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(iii) STATUS OF CLAIMS

Claims 1-27 are pending in this application. Claims 1-27 have been finally rejected and form the basis for the appeal.

(iv) STATEMENT OF AMENDMENTS

A Final Office Action was mailed on September 20, 2005, in which Claims 1-27 were rejected under 35 U.S.C. §103(a) as unpatentable over Odryna et al. (U.S. Patent No. 6,333,750, herein "Odryna") in view of Glen (U.S. Patent No. 6,157,415, herein "Glen '415") and Glen (U.S. Patent No. 6,268,847, herein "Glen '847"). In response, a Notice of Appeal was filed on December 20, 2005.

(v) SUMMARY OF CLAIMED SUBJECT MATTER

Display devices, such as projectors, are capable of simultaneously displaying image signals from different types of devices providing images. For example, these display devices are capable of simultaneously displaying images played from a video cassette recorder, a video camera, etc, and can be superimposed over an image or graphics provided from a personal computer. The superimposing of images, such as the video signals, over a single reference image is called "overlaying."

Appellants of the present invention have realized that many display devices are not capable of arbitrarily selecting the reference image for overlaying, accordingly they have provided by the present invention an overlay image processing device and a method for generating an overlay image signal, where a reference image can be arbitrarily selected for the overlaying.

As shown in a non-limiting illustration in Figures 1 and 2, of Appellants' Specification, the invention as recited in independent Claim 1 is directed to an overlay image processing device for generating an overlay image signal composed of an n number of selected image signals, n being an integer greater than 2.[1] The overlay image processing device includes: a plurality of digital decoders 110, 112, 114[2] configured to digitally decode a plurality of image signals VPC(A), VS1(A), VS2(A);[3] an image selector 116 configured to directly receive outputs from each of the plurality of digital decoders 110, 112, 114,[4] and configured to select from among the plurality of digitally decoded image signals one reference image signal SD10 and n-1 number of superimposing image signals SD20;[5] a plurality of resolution converters 118, 120 configured to directly receive the selected image

[1] See Appellants' specification at page 9, lines 11-14 and in Figures 8A-8F.
[2] Idem at page 4, lines 18-19.
[3] Idem at page 5, lines 12-20.
[4] Idem at page 6, lines 18-20.
[5] Idem at page 6, lines 20-24.

signals output from the image selector,[6] such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective adjustable desired resolutions,[7] and to output the converted image signals to an image synthesizer 130,[8] wherein the image synthesizer 130 is configured to superimpose the n-1 number of converted superimposing image signals SD20 on the converted one reference signal SD10, and the image selector 116 is configured to connect each of the digital decoders to any of the resolution converters 118, 120.

Independent Claims 11 and 20 recite similar features as method claims. Support for the claimed steps of Claim 11 appears in the functions performed by the plurality of digital decoders 110, 112, 114[9] (digitally decoding), the outputs of the digital decoders 110, 112, 114 directly linked to the selector 116[10] (directly inputting), by the image selector 116[11] (selecting), by a plurality of resolution converters 118, 120 (converting resolutions), and by the image synthesizer 130 (superimposing). Support for the claimed steps of Claim 20 appears in the functions performed by the outputs of the digital decoders 110, 112, 114 directly linked to the selector 116[12] (inputting), by a plurality of resolution converters 118, 120 (converting resolutions), the two overlay processors 130, 132[13] (first and second superimposing).

Independent Claim 6 recites an overlay image processing device with analogous features as claimed in Claim 1, and additionally recites an image display device for displaying an image.[14]

---

[6] Idem at page 6, lines 25-30.
[7] Idem at page 4, line 19.
[8] Idem at page 7, lines 10-13.
[9] Idem at page 4, lines 18-19.
[10] Idem at page 6, lines 12-24 and in Figure 2.
[11] Idem at page 6, lines 18-24 and in Figure 2.
[12] Idem at page 6, lines 12-24 and in Figure 2.
[13] Idem at page 12, lines 24-28 and in Figure 11.
[14] Idem Figure 1.

Independent Claim 16 recites analogous features to Claim 1 without positively claiming the digital decoders 110, 112, 114 and the image synthesizer 130.

(vi) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds for rejection to be reviewed on appeal and outstanding in the present application are as follows:

Claims 1-27 were rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. Odryna et al. (U.S. Patent No. 6,333,750, herein "Odryna"), in view of Glen (U.S. Patent No. 6,157,415, herein "Glen '415") and Glen (U.S. Patent No. 6,268,847, herein "Glen '847").

(vii) ARGUMENT

Appellants respectfully submit that none of the references, Odryna, Glen '415 and Glen '847, teach or suggest an image selector configured to *directly receive outputs from each of the plurality of digital decoders*, wherein the image selector is configured to connect each of the digital decoders to any of the resolution converters, as next discussed.

The outstanding Office Action asserts that Odryna teaches the Claim 1 image selector[15] relative to various elements of Odryna's Figures 17, 18 and 21 considered together and apart from the context in which Odryna discloses the elements to be connected and operated. In particular, the outstanding Office Action points to control block 111 (Figure 18) inside a system card 110 (Figure 18) accessing a signal control bus 113, the control array 188 and the memories 186 (Figure 21), and also points to the inputs A-C (Figure 17), all together being elements that, if combined and modified, would read-upon Appellants' Claim 1 image selector. Furthermore, the outstanding Office Action argues that all the control arrays [188]

[15] See the outstanding Office Action, from page 2, line 14 to page 3, line 12, and from page 9, line 18 to page 10, line 8, as well as at page 11, lines 8-13.

"are programmed by the control block 111 of the system card 110 via the serial control bus 113 to control the overlay of the base image with other images."[16] However, Odryna explicitly states that the control block 111 includes serial interfaces to configure interface cards of the Figure 17 hub,[17] for example, to instruct output of an appropriate pixel data onto the pixel bus 114,[18] and analyzes the HSYNC and VSYNC from an incoming video signal to identify the source.[19] Accordingly, the control block 111 is merely programmed to control an input card to provide overlay data to the bus, and does not have the function of the claimed image selector as the system card 110 does not "directly receive inputs from each of the plurality of digital decoders" as specified in Claim 1. The outstanding Action admits that the digital decoders are in the input cards (A-C of Figure 17), not in card 110.

Even though the Figure 17 teaching of Odryna belongs clearly to a separate system card 110 and input cards A-C, the outstanding Action suggests that these separate elements would somehow be combined together to perform as the Claim 1 image selector. However, the outstanding Action fails to point to any teaching or suggestion in Odryna suggesting the arrangement and operation of the FIG. 17 hub should be so modified. Motivation for modifying even a single reference arrangement of elements to a new arrangement of elements must be shown. See *B.F. Goodrich Co. v. Aircraft Braking Sys. Corp.*, 72 F.3d 1577, 1582, 37 USPQ2d 1314, 1318 (Fed. Cir. 1996). In this last regard, motivation is required not only to show a reason why card 110 and the input cards A-C would have been combined but also why the digital decoders would be removed from the input cards so that they could then meet the Claim 1 requirement for digital decoders that will supply their outputs directly to the image selector of Claim 1.

[16] Idem at page 3, lines 5-7 and page 10, lines 1-3.
[17] See Odryna at column 18, lines 1-7.
[18] See Odryna at column 17, lines 39-45.
[19] See Odryna at column 18, lines 30-34, and in corresponding Figure 18.

Moreover, the proposed combination of Odryna, Glen '415 and Glen '847 references does not teach the claimed plurality of resolution converters *configured to directly receive the selected image signals output from the image selector*, such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective *adjustable desired resolutions*.

The outstanding Office Action asserts that Odryna's scaler 184 reads upon Appellants' resolution converter.[20] However, Odryna explicitly teaches that the broadcast video "decoder [182] provides the video data in digital form to a scaler 184," and also teaches that in an alternative embodiment, "the scaler 184 is utilized at the output of the buffer memory 186."[21] Accordingly, a scaler 184 receiving data either from a video decoder or from a buffer memory 186 of a control array 188, as clearly described in Odryna, ***is not*** a resolution converter configured to directly receive the selected image signals output ***from the image selector***, as claimed by Appellants. These elements (182, 184, 186, 188) are all inside the BVIDEO overlay card 180.[22] In order to have these elements receive image signals from the image selector, they must be removed from the card that is part of the argued image selector.

The only attempt to explain why the artisan would have combined the cards in Figure 17 appears at page 4, lines 7-12, and page 13, lines 7-12, of the outstanding Action. This explanation is based on the Larsen and Wolfe cases and appears to suggest that the U.S.P.T.O. is interpreting these cases to say it is always obvious to make an integral element from a plurality of disclosed individual elements. This interpretation is clearly erroneous.

In the cited Larsen case, the brake assembly at issue was shown by a reference to be made of several parts that were rigidly secured together as a "single unit." This showing was

[20] See the outstanding Office Action at page 3, lines 9-15, and at page 10, lines 9-20, pointing out to Odryna's Figures 17 and 21.
[21] See Odryna in Figure 21 and in the specification from column 20, line 52, to column 21, line 7.
[22] See Odryna at column 20, lines 44-51 and in Figures 20 and 21.

found by the court to be "integral," which is not the same thing as suggesting that no motivation need be shown as to integrating separate loose parts into a "single unit."

The Wolfe case seems more on point as the decision states that making a two-piece handle in one piece would have been obvious. However, the plurality of cards here are not handle parts and the removal of the video decoder and the scaler from the input cards goes for beyond simply combining like elements into an integrated whole.

The reference Glen '415 does not remedy the deficiencies of Odryna. However, the outstanding Office Action asserts that Glen '415's color base converting module 102 and blend module 76, 78, 80 read upon the claimed resolution converters.[23] As explained in Glen '415, each of the blend modules 76, 78, 80 receives different image signals in one of three predetermined formats, i.e., RGB, HDTV, and TV, and then outputs a single image signal in another one of the same three predetermined formats.[24] However, a color conversion module to convert a color base and a image blending module to merge images together, as taught by Glen '415, ***is not*** a resolution converters *configured to directly receive the selected image signals output from the image selector.*

The reference Glen '847 is also concerned with color base conversion, between YUV and RGB data,[25] and is also silent on Appellants' claimed features regarding a resolution converter.

Therefore, even if the combination of the Odryna, Glen '415 and Glen '847 is assumed to be proper, the combination fails to teach every element of the claimed invention. Accordingly, Appellants respectfully request reversal of this rejection based on these references.[26]

---

[23] See the outstanding Office Action from page 6, line 18 to page 7, line 3 and at page 15, lines 5-12.
[24] See Glen '415 from column 5, line 50 to column 6, line 15.
[25] See Glen '847 in the Abstract and in Figure 1.
[26] See MPEP 2142 stating, as one of the three "basic criteria [that] must be met" in order to establish a *prima facie* case of obviousness, that "the prior art reference (or references when combined) must teach or suggest all

Appellants further respectfully submit that the outstanding Office Action seems to point to different elements of the references Odryna, Glen '415 and Glen '847 and to make new interconnections between the different elements, and to set up new data flows, none of which are taught by the reference. Such a rationale is clearly one using improper hindsight. Even if it may be true that the different elements can perform a certain function if they would have been interconnected and programmed to perform such a function, these interconnections and programs for data flows must be taught or suggested by Odryna, Glen '415 and Glen '847, taken individually or in combination, not simply be possibilities offered by the U.S.P.T.O. The outstanding Office Action seems to use improper hindsight by rejecting Appellants' claims by constructing a solution based on the teachings of Appellants' claims. See In re Lowry, 32 F.3d 1579, 1583 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) to recite "[t]o establish a prima facie case of obviousness, the burden of establishing the absence of a novel, nonobvious functional relationship rested with the Patent and Trademark Office," and "[t]he claimed invention involved an organization of information and its interrelationships that the prior invention neither disclosed nor suggested." See also Monarch Knitting Mach. Corp. v. Sulzer Morat Gmbh, 139 F.3d 877, 880, 45 USPQ2d 1977, 1981 (Fed. Cir. 1998) "[d]efining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness."

Moreover, in order to modify Odryna as suggested by the U.S.P.T.O., it is clear that there would be a substantial redesign of the card of Odryna and a surgical removal of selected elements (such as the decoders) that would result in a change of the basic operation of these cards of Odryna. Such modifications are not considered obvious ones, see In re Ratti, 270 F.2d 810, 813, 123 USPQ 349, 352 (CCPA 1959).

---

the claim limitations," (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."

Appellants further respectfully traverse the suggestion that there is a showing of evidence of motivation to modify the Odryna video input cards connected to a video data hub for video distribution,[27] by incorporating Glen '415's image blending and color base conversion modules,[28] for the following reasons.[29]

The outstanding Office Action states that it would have been obvious to "incorporate[d] a different circuit configuration ... for example, the circuit configuration of Glen-415 reference wherein the image selector is used to connect each of the decoder output signals or input image signals to any of the resolution converters, into Odryna's system because Odryna's system is highly reconfigurable with instructions from the programmable controller such as the system card."[30] However, Appellants believe that one skilled in the art would not be motivated to make the proposed modification because the integration of Glen '415's switch matrix 140[31] or configuration module 40[32] would render Odryna's video graphics systems unsatisfactory for its intended purpose; and would change the principle operation of Odryna's system. More particularly, by directing signals from each of Odryna's decoders 182 (e.g., of input card A) to any scaler 184 (e.g., of input card C), through Glen '415's switch matrix 140, the proposed modification would obviate the intended integration of signal decoding and conversion of an input signal within a single input card, to deliver image data to a pixel bus 14 for later displaying.[33] In fact, the proposed modification would require the passing of an input signal amongst multiple "input" cards A-C. Odryna's Figure

---

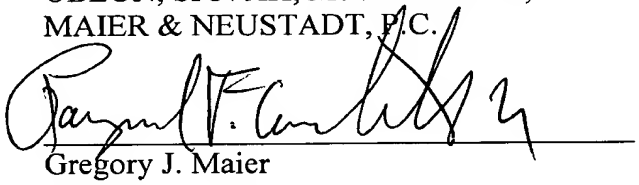
[27] See Odryna in the Abstract.
[28] See Glen '415 in the Abstract.
[29] See MPEP 2143.01 stating "[o]bviousness can only be established by combining or modifying the teaching of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art," (citations omitted). See also MPEP 2144.08 III stating that "[e]xplicit findings on motivation or suggestion to select the claimed invention should also be articulated in order to support a 35 U.S.C. 103 ground of rejection. . . Conclusory statements of similarity or motivation, without any articulated rational or evidentiary support, do not constitute sufficient factual findings."
[30] See outstanding Office Action at page 8, lines 1-7, and at page 17, lines 11-17.
[31] See Glen '415 in Figure 9, reference numeral 140.
[32] See Glen '415 in Figure 9, reference numeral 40.
[33] See Odryna at column 2, lines 28-54.

17 precludes such a passing of signals amongst the input cards. Such modification would require a substantial reconstruction or redesign of the elements of Odryna, and/or would change the basic principle of operation of Odryna. There is again no evidence that a person of ordinary skill in the art would be motivated to perform such changes and redesign that one contrary to the above-noted Ratti decision. Thus, for instance, a scaler 184 can process a signal input to its respective card, but the same scaler 184 cannot process a signal input to another input card. Appellants again believe that the outstanding Office Action is basing the rejection on improper hindsight in terms of constructing a new system without support for all the elements and their interconnections in the relied upon references.

In view of these foregoing comments regarding independent Claims 1, 6, 11, 16 and 20, and as claims depend from these independent claim and include these limitations, it is respectfully submitted that each of the pending Claims 1-27 clearly distinguish over the applied art, and thus the outstanding rejection of Claims 1-27 should be REVERSED.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599

Raymond F. Cardillo, Jr.
Registration No. 40,440

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

I:\ATTY\NS\004947\204155US\204155US.APPEAL BRIEF-DRAFT 3.DOC

(viii) CLAIMS APPENDIX

Claim 1: An overlay image processing device for generating an overlay image signal composed of an n number of selected image signals, n being an integer greater than 2, the overlay image processing device comprising:

a plurality of digital decoders configured to digitally decode a plurality of image signals;

an image selector configured to directly receive outputs from each of the plurality of digital decoders and configured to select from among the plurality of digitally decoded image signals one (1) reference image signal and (n-1) number of superimposing image signals;

a plurality of resolution converters configured to directly receive the selected image signals output from the image selector, such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective adjustable desired resolutions, and to output the converted image signals to an image synthesizer,

wherein the image synthesizer is configured to superimpose the (n-1) number of converted superimposing image signals on the converted one (1) reference signal, and

the image selector is configured to connect each of the digital decoders to any of the resolution converters.

Claim 2: An overlay image processing device according to claim 1 wherein at least one of the plurality of image signals is a display signal output from a personal computer.

Claim 3: An overlay image processing device according to claim 1 wherein the image selector selects the reference image signal and the (n-1) number of superimposing image

signals according to an arbitrary predetermined order of superposition for the n number of image signals; and

the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition.

Claim 4: An overlay image processing device according to claim 1 further comprising a scan converter configured to convert at least one of the interlaced image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

Claim 5: An overlay image processing device according to claim 1 wherein the image synthesizer has the n number of 2-input image synthesizers, each 2-input image synthesizer being configured to receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal;

the n number of 2-input image synthesizers being connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of an i^{th} stage, where i is between 2 and n, inclusive, uses an output of the 2-input image synthesizer of an $(i-1)^{th}$ stage as the lower-side image signal and an i^{th} superimposing image signal as the upper-side image signal.

Claim 6: An overlay image display device for displaying an overlay image composed of an n number of selected images, n being an integer greater than 2, the overlay image display device comprising:

an overlay image processing device for generating an overlay image signal composed of the n number of superimposed image signals; and

an image display device for displaying an image represented by the overlay image signal;

wherein the overlay image processing device includes:

a plurality of digital decoders configured to digitally decode a plurality of image signals;

an image selector configured to directly receive outputs from each of the plurality of digital decoders and configured to select from among the plurality of digitally decoded image signals one (1) reference image signal and (n-1) number of superimposing image signals;

a plurality of resolution converters configured to directly receive the selected image signals output from the image selector, such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective adjustable desired resolutions, and to output the converted signals to an image synthesizer,

wherein the image synthesizer is configured to superimpose the (n-1) number of converted superimposing image signals on the converted one (1) reference signal, and

the image selector is configured to connect each of the digital decoders to any of the resolution converters.

Claim 7: An overlay image display device according to claim 6 wherein at least one of the m number of image signals is a display signal output from a personal computer.

Claim 8: An overlay image display device according to claim 6 wherein the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and

the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition.

Claim 9: An overlay image display device according to claim 6 further comprising a scan converter configured to convert at least one of the image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

Claim 10: An overlay image display device according to claim 6 wherein the image synthesizer has the n number of 2-input image synthesizers, each 2-input image synthesizer being configured to receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal;

the n number of 2-input image synthesizers being connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of an i^{th} stage, where i is between 2 and n, inclusive, uses an output of the 2-input image synthesizer of an $(i-1)^{th}$ stage as the lower-side image signal and an i^{th} superimposing image signal as the upper-side image signal.

Claim 11: A method of generating an overlay image signal composed of an n number of superimposed image signals, n being an integer greater than 2, the method comprising the steps of:

(a) digitally decoding a plurality of image signals by use of a plurality of respective digital decoders;

(b) directly inputting outputs from each of the plurality of digital decoder to an image selector;

(c) selecting from among the plurality of digitally decoded image signals, by use of the image selector, one (1) reference image signal and (n-1) number of superimposing image signals;

(d) converting resolutions of the n number of selected image signals received directly from the image selector, including the reference image signal and the (n-1) number of superimposing image signals, into respective adjustable desired resolutions by use of a plurality of resolution converters directly receiving respective outputs of the of the image selector, such that any resolution converter can receive any output of the image selector; and

(e) superimposing the (n-1) number of converted superimposing image signals on the converted reference signal,

wherein an output of step (d) is output to step (e), and

each of the digital decoders can be connected to any of the resolution converters via the image selector.

Claim 12: A method according to claim 11 wherein at least

one of the plurality of image signals is a display signal output from a personal computer.

Claim 13: A method according to claim 11 wherein the step (c) includes selecting the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and

the step (e) includes superimposing the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition.

Claim 14: A method according to claim 11 further comprising converting at least one of the image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

Claim 15: A method according to claim 11 wherein the step

(e) includes the n number of 2-input image synthesizing steps, each 2-input image synthesizing step including receiving upper-side and lower-side image signals and superimposing an upper-side image signal on a lower-side image signal;

the n number of 2-input image synthesizing steps being performed in series in multistage fashion such that the 2-input image synthesizing step of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizing step of an i^{th} stage, where i is between 2 and n, inclusive, uses an output of the 2-input image synthesizing step of an $(i-1)^{th}$ stage as the lower-side image signal and an i^{th} superimposing image signal as the upper-side image signal.

Claim 16: An overlay image processing device for generating an overlay image signal composed of an n number of selected image signals, n being an integer greater than 2, the overlay image processing device comprising:

an image selector configured to select, from among a plurality of image signals received directly from a plurality of respective digital decoders, one (1) reference image signal and (n-1) number of superimposing image signals;

a plurality of resolution converters configured to directly receive the selected image signals output from the image selector, such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective adjustable desired resolutions, and to output the converted image signals to an image synthesizer,

wherein the image synthesizer is configured to superimpose the (n-1) number of converted superimposing image signals on the converted one (1) reference signal, the image synthesizer includes first and second overlay processors connected in series, the first overlay processor is configured to receive an output from a subset of the plurality of resolution converters, and the second overlay processor is configured to directly receive an output from the first overlay processor and another of the plurality of resolution converters, and the image selector is configured to connect each of the digital decoders to any of the resolution converters.

Claim 17: An overlay image processing device according to claim 16 wherein at least one of the plurality of image signals is a display signal output from a personal computer.

Claim 18: An overlay image processing device according to claim 16 wherein the image selector selects the reference image signal and the (n-1) number of superimposing

image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and

the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition.

Claim 19: An overlay image processing device according to claim 16 further comprising a scan converter configured to convert at least one of the interlaced image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

Claim 20: A method of generating an overlay image signal composed of an n number of selected image signals, n being an integer greater than 2, the method comprising the steps of:

(a) inputting a plurality of image signals directly from a plurality of respective digital decoders to an image selector and selecting one (1) reference image signal and (n-1) number of superimposing image signals from among the plurality of image signals;

(b) converting resolutions of the n number of selected image signals, including the reference image signal and the (n-1) number of superimposing image signals, into respective adjustable desired resolutions by use of a plurality of resolution converters directly inputting respective outputs of the image selector, such that any resolution converter can receive any output of the image selector; and

(c) first superimposing the (n-1) number of converted superimposing image signals on the converted reference signal, the first superimposing receiving an output from a subset of a plurality of steps (b); and

(d) second superimposing a directly received output from the first overlay processor and another output of the plurality of steps (b),

wherein an output of step (b) is output to step (e), and

each of the digital decoders can be connected to any of the resolution converters via the image selector.

Claim 21: A method according to claim 20 wherein at least one of the plurality of image signals is a display signal output from a personal computer.

Claim 22: A method according to claim 20 wherein the step (a) includes selecting the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and

the steps (c) and (d) include superimposing the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition.

Claim 23: A method according to claim 20 further comprising converting at least one of the image signals selected by step (a) into a non-interlaced image signal when the at least one of the image signals selected by step (a) is an interlaced image signal.

Claim 24: An overlay image processing device according to claim 6,

wherein the respective outputs of the image selector include an analog RGB signal and a horizontal sync signal,

wherein each of the resolution converters generates a clock signal synchronized with the horizontal sync signal and corresponding to a pixel clock for the analog RGB signal, and

quantizes the RGB signal in synchronism with the clock signal to convert the analog RGB signal to a digital RGB signal, and

wherein a single image signal element quantized by each of the resolution converters corresponds to one pixel of the image represented by the RGB signal.

Claim 25: A method of generating an overly image signal according to Claim 11, wherein the step (d) of converting resolutions further includes the steps of:

(i) inputting an analog RGB signal and a horizontal sync signal;

(ii) outputting a clock signal that is synchronized with the horizontal sync signal and corresponds to a pixel clock for the analog RGB signal;

(iii) converting the analog RGB signal to a digital RGB signal by quantizing the analog RGB signal in synchronism with the clock signal; and

(iv) changing the resolution of the image represented by the quantized RGB signal by changing the frequency of the clock signal.

Claim 26: An overlay image processing device according to claim 16,

wherein the respective outputs of the image selector include an analog RGB signal and a horizontal sync signal,

wherein each of the resolution converters generates a clock signal synchronized with the horizontal sync signal and corresponding to a pixel clock for the analog RGB signal and quantizes the RGB signal in synchronism with the clock signal to convert the analog RGB signal to a digital RGB signal, and

wherein a single image signal element quantized by each of the resolution converters corresponds to one pixel of the image represented by the RGB signal.

Claim 27: A method of generating an overly image signal according to Claim 20, wherein the step (b) of converting resolutions further includes the steps of:

(i) inputting an analog RGB signal and a horizontal sync signal;

(ii) outputting a clock signal that is synchronized with the horizontal sync signal and corresponds to a pixel clock for the analog RGB signal;

(iii) converting the analog RGB signal to a digital RGB signal by quantizing the analog RGB signal in synchronism with the clock signal; and

(iv) changing the resolution of the image represented by the quantized RGB signal by changing the frequency of the clock signal.

(ix) EVIDENCE APPENDIX

None.

(x) RELATED PROCEEDINGS APPENDIX

None.